AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-11. (Canceled)

12. (Currently Amended) A flash memory comprising:

a plurality of array planes that constitute all storage corresponding to a logical address space of the Flash memory, each array plane including:

a plurality of blocks of memory cells, wherein the blocks store parameters, code, and data, and all the blocks in the array planes have a uniform size selected for parameter storage, wherein the blocks include:

memory blocks having respective physical addresses that correspond to logical addresses of the Flash memory; and

spare memory blocks having respective physical addresses that do not correspond to the logical addresses of the Flash memory; and

a redundancy information block of the array plane, storing therein defect addresses identifying memory blocks having defective memory elements within the array plane and substitute addresses for spare memory blocks replacing the memory blocks having the defective memory elements;

a content addressable memory array coupled to the redundancy information blocks of the plurality of array planes to receive therefrom the defect addresses, and also being coupled to receive a logical signal from an external device for comparison with the defect addresses stored in the content addressable memory array;

a memory array coupled to the redundancy information blocks of the plurality of array planes to receive therefrom the substitute addresses, and also having word lines coupled to respective match lines of the content addressable memory array,

wherein in response to activation of one of the match lines, the memory array outputs a substitute address signal representing [[a]] one of the substitute ~~address~~ addresses stored in a row corresponding to the activated match line; and

multiplexing circuitry connected to select between the logical address signal and the substitute address signal as a physical address signal, the multiplexing circuitry providing the physical address signal for selection of a memory cell being accessed.

13. (Currently Amended) The memory of claim 12, wherein each of the blocks comprises 4-Kword blocks of memory cells that are connected to permit simultaneous erasure of all of the memory cells in the block.

14. (Currently Amended) The memory of claim 13, further comprising:

a write data path; and

a read data path, wherein

the array planes are connected to the write data path and the read path so as to permit any one of the array planes to conduct a read operation while any other of the array planes conducts a write operation.

15. (Previously Presented) The memory of claim 14, wherein each array plane contains erase circuitry that permits the array plane to erase a block in the array plane, while other array planes conduct read and write operations.

16. (Previously Presented) The memory of claim 14, wherein each array plane comprises at least one of the spare memory blocks.

17. (Original) The memory of claim 16, wherein each array plane comprises a spare global bit line that connects to all blocks in the array plane.

18. (Previously Presented) An operating method for a Flash memory[[,]] having a plurality of array planes, the method comprising:

storing parameters, code, and data in separate blocks of memory cells, wherein each of the blocks has a uniform size selected for parameter storage;

storing defect addresses in a content addressable memory array in the Flash memory;

storing substitute addresses in a substitute address memory array in the Flash memory;

applying a first logical address from an external device to the content addressable memory array for a comparison operation;

outputting from the substitute address memory array a substitute address corresponding to a match line activated as a result of the comparison operation; and

accessing one of the blocks corresponding to the substitute address instead of another block corresponding to the first logical address.

19. (Original) The method of claim 18, further comprising applying a second logical address from the external device directly to a decoder in the Flash memory while applying the first logical address to the content addressable memory, wherein a combination of the first and second logical addresses identifies a memory cell.

20. (Currently Amended) ~~The method of claim 19,~~ An operating method for a Flash memory, comprising:

storing parameters, code, and data in separate blocks of memory cells, wherein each of the blocks has a uniform size selected for parameter storage;

storing defect addresses in a content addressable memory array in the Flash memory;

storing substitute addresses in a substitute address memory array in the Flash memory;

applying a first logical address from an external device to the content addressable memory array for a comparison operation;

applying a second logical address from the external device directly to a decoder in the Flash memory while applying the first logical address to the content addressable memory, wherein a combination of the first and second logical addresses identifies a memory cell;

outputting from the substitute address memory array a substitute address corresponding to a match line activated as a result of the comparison operation; and

accessing one of the blocks corresponding to the substitute address instead of another block corresponding to the first logical address,

wherein the first logical address is a block address and the second logical address identifies a memory cell within a block.

21. (Original) The method of claim 20, wherein the second logical address is a row address.

22. (Currently Amended) The method of claim 18, wherein accessing ~~the memory element~~ one of the blocks comprises accessing a first array plane in the Flash memory while a second array plane in the Flash memory conducts a second operation.

23. (Original) The method of claim 22, wherein accessing the first array plane comprises reading a memory cell in the first array plane, and the second operation comprises writing to a memory cell in the second array plane.

24. (Original) The method of claim 22, wherein accessing the first array plane comprises reading a memory cell in the first array plane, and the second operation comprises erasing a block in the second array plane.

Claims 25-26. (Canceled)

27. (New) The method of claim 18, wherein storing defect addresses in a content addressable memory array in the Flash memory and storing substitute addresses in a memory array in the Flash memory, comprises:

storing the defect addresses and substitute addresses for each array plane in a corresponding redundancy information block of each array plane;

transferring the defect addresses from the redundancy information block of each array plane to the content addressable memory array; and

transferring the substitute addresses from the redundancy information block of each array plane to the substitute address memory array.

28. (New) The method of claim 27, wherein transferring the defect addresses from the redundancy information block of each array plane to the content addressable memory array and transferring the substitute addresses from the redundancy information block of each array plane to the substitute address memory array occurs during a power up operation of the Flash memory.